

IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A method for fabricating an integrated circuit, comprising the steps of:

fabricating a portion of [[an]] the integrated circuit, the portion comprising at least one active circuit area; and

fabricating a redistribution metal layer ~~in said integrated circuit~~ at least partially during [[a]] fabrication ~~process~~ of said the portion of said the integrated circuit.

2. (Currently Amended) The method as set forth in Claim 1, wherein fabricating the redistribution metal layer comprises ~~further comprising~~ the step of:

fabricating portions of ~~said~~ the redistribution metal layer that are open to receive a solder bump.

3. (Currently Amended) The method as set forth in Claim 1, wherein fabricating the portion of the integrated circuit and the redistribution metal layer comprises ~~further comprising the steps of:~~

fabricating ~~[[an]]~~ the active circuit area and an associated metal pad on a base substrate;

fabricating a vertical plug ~~of a redistribution metal layer;~~

mounting ~~said~~ the vertical plug ~~of said redistribution metal layer on said metal pad; in electrical connection with the electrically connecting said vertical plug of said redistribution metal layer to said metal pad;~~

depositing an undoped silicon oxide layer on ~~said~~ the active circuit area and on a portion of the said metal pad;

depositing a phosphosilicate glass layer on ~~said~~ the undoped silicon oxide layer;

depositing a silicon oxynitride layer over ~~said~~ the phosphosilicate glass layer; and

depositing a flat ~~redistribution~~ metal layer over ~~said~~ the silicon oxynitride layer ~~[[;]]~~ and in electrical connection with the electrically connecting said flat redistribution metal layer to said vertical plug of said redistribution metal layer.

4. (Currently Amended) The method as set forth in Claim 3, wherein fabricating the redistribution metal layer further comprises ~~further comprising~~ the steps of:

depositing a polyimide layer over portions of ~~said~~ the flat ~~redistribution~~ metal layer and over portions of ~~said~~ the silicon oxynitride layer; and

etching portions of ~~said~~ the polyimide layer to leave portions of ~~said~~ the flat ~~redistribution~~ metal layer open to receive a solder bump.

5. (Currently Amended) The method as set forth in Claim 1, wherein fabricating the portion of the integrated circuit and the redistribution metal layer comprises ~~further comprising~~ the steps of:

fabricating ~~[[an]]~~ the active circuit area and an associated metal pad on a base substrate;

depositing an undoped silicon oxide layer on ~~said~~ the active circuit area and on ~~said~~ at least a portion of the metal pad;

depositing a phosphosilicate glass layer on ~~said~~ the undoped silicon oxide layer;

depositing a ~~redistribution~~ metal layer over ~~said~~ the phosphosilicate glass layer ~~[[;]]~~ and in electrical connection with the ~~electrically connecting said redistribution metal layer to said~~ metal pad; and

depositing a silicon oxynitride layer over at least some portions of ~~the said redistribution~~ metal layer.

6. (Currently Amended) The method as set forth in Claim 5, wherein fabricating the redistribution metal layer further comprises ~~further comprising~~ the step of:
leaving portions of ~~the said redistribution~~ metal layer open to receive a solder bump.

7. (Currently Amended) The method as set forth in Claim 5, wherein depositing the silicon oxynitride layer comprises ~~further comprising~~ the step of:
depositing a silicon oxynitride layer over all portions of ~~the said redistribution~~ metal layer.

8. (Currently Amended) The method as set forth in Claim 7, wherein fabricating the redistribution metal layer further comprises ~~further comprising~~ the step of:
etching ~~said~~ the silicon oxynitride layer to a pattern that leaves portions of ~~the said redistribution~~ metal layer uncovered to receive a solder bump.

9. (Currently Amended) The method as set forth in Claim 5, wherein fabricating the redistribution metal layer further comprises ~~further comprising~~ the steps of:
depositing a polyimide layer over portions of ~~the said redistribution~~ metal layer and over portions of ~~said~~ the silicon oxynitride layer; and
etching portions of ~~said~~ the polyimide layer to leave portions of ~~said the flat redistribution~~ metal layer open to receive a solder bump.

10. (Currently Amended) The method as set forth in Claim 1, wherein fabricating the redistribution metal layer comprises ~~further comprising~~ the step of:

fabricating ~~said~~ the redistribution metal layer using a last metal layer that is used to fabricate ~~[[an]]~~ the active circuit area of ~~said~~ the integrated circuit.

11. (Currently Amended) An integrated circuit, comprising:
a portion ~~of an integrated circuit~~ comprising at least one active circuit area; and
a redistribution metal layer ~~in said integrated circuit~~ fabricated at least partially during ~~[[a]]~~ fabrication ~~process~~ of ~~said~~ the portion of ~~said~~ the integrated circuit.

12. (Currently Amended) The integrated circuit as set forth in Claim 11, wherein portions of ~~said~~ the redistribution metal layer in ~~said~~ the integrated circuit are open to receive a solder bump.

13. (Currently Amended) The integrated circuit as set forth in Claim 11, wherein the portion of the integrated circuit and the redistribution metal layer comprise further comprising:

[[an]] the active circuit area and an associated metal pad on a base substrate;

a vertical plug ~~of a redistribution metal layer~~ mounted on and electrically connected to ~~said the~~ metal pad;

~~a layer of an~~ undoped silicon oxide layer deposited on ~~said the~~ active circuit area and on a portion of the said metal pad;

a phosphosilicate glass layer deposited on ~~said the~~ undoped silicon oxide layer;

a silicon oxynitride layer deposited on ~~said the~~ phosphosilicate glass layer; and

a flat ~~redistribution~~ metal layer deposited over ~~said the~~ silicon oxynitride layer;

wherein ~~said the~~ flat ~~redistribution~~ metal layer is electrically connected to ~~said the~~ vertical plug ~~of said redistribution metal layer~~.

14. (Currently Amended) The integrated circuit as set forth in Claim 13, wherein the redistribution metal layer further comprises comprising:

a polyimide layer deposited over portions of ~~said the~~ flat ~~redistribution~~ metal layer and over portions of ~~said the~~ silicon oxynitride layer;

wherein ~~said the~~ polyimide layer is etched to leave portions of ~~said the~~ flat ~~redistribution~~ metal layer open to receive a solder bump.

15. (Currently Amended) The integrated circuit as set forth in Claim 11, wherein the portion of the integrated circuit and the redistribution metal layer comprise further comprising:

[[an]] the active circuit area and an associated metal pad on a base substrate;

an undoped silicon oxide layer deposited on ~~said~~ the active circuit area and on ~~said~~ at least a portion of the metal pad;

a phosphosilicate glass layer deposited on ~~said~~ the undoped silicon oxide layer;

a ~~redistribution~~ metal layer deposited over ~~said~~ the phosphosilicate glass layer, wherein ~~said redistribution~~ the metal layer is electrically connected to ~~said~~ the metal pad; and

a silicon oxynitride layer deposited over at least some portions of ~~said~~ the ~~redistribution~~ metal layer.

16. (Currently Amended) The integrated circuit as set forth in Claim 15, wherein portions of ~~said redistribution~~ the metal layer are open to receive a solder bump.

17. (Currently Amended) The integrated circuit as set forth in Claim 15, wherein the silicon oxynitride layer comprises further comprising:

a silicon oxynitride layer deposited over ~~said redistribution~~ all portions of the metal layer and etched to a pattern that leaves portions of ~~said redistribution~~ the metal layer uncovered to receive a solder bump.

18. (Currently Amended) The integrated circuit as set forth in Claim 15,
wherein the redistribution metal layer further comprising comprises:

a polyimide layer deposited over portions of ~~said redistribution~~ the metal layer and over
portions of ~~said~~ the silicon oxynitride layer;

wherein portions of ~~said redistribution~~ the metal layer are open to receive a solder bump.

19. (Currently Amended) The integrated circuit as set forth in Claim 11,
wherein the redistribution metal layer comprises further comprising:

a redistribution metal layer fabricated using a last metal layer that is used to fabricate
[[an]] the active circuit area of ~~said~~ the integrated circuit.

20. (Currently Amended) The integrated circuit as set forth in Claim 12,
further comprising:

a solder bump attached to ~~said~~ the portions of ~~said~~ the redistribution metal layer ~~of said~~
~~integrated circuit~~ that are open to receive a solder bump.

21. (Currently Amended) The integrated circuit as set forth in Claim 14,
further comprising:

a solder bump attached to ~~said~~ the portions of ~~said~~ the flat ~~redistribution~~ metal layer ~~of~~
~~said integrated circuit~~ that are open to receive a solder bump.

22. (Currently Amended) The integrated circuit as set forth in Claim 16,
further comprising:
a solder bump attached to ~~said~~ the portions of ~~said~~ the flat redistribution metal layer of
~~said integrated circuit~~ that are open to receive a solder bump.

Claims 23-30 (Cancelled).